REMARKS

In response to the Official Action mailed April 29, 2002, Applicants have amended Claim 2 to place Claim 2 in independent form. Applicants have also amended Claim 1 to clarify that the first oxide layer is provided directly on the SiC region. Applicants have cancelled Claim 32 and amended Claim 33 to write Claim 33 in independent form. Finally, Applicants have canceled the non-elected Claims 22-31 and 47-56. In light of the discussion below, Applicants submit that the present application is in condition for allowance.

The Double Patenting Rejection

Claims 1-21 stand rejected based on the judicially created doctrine of obviousness-type double patenting. Official Action, p. 2. Applicants respectfully defer addressing such rejection until such time as any one of Claims 1-21 are considered patentable except for such rejection. If such is the case, Applicants will timely submit a terminal disclaimer to overcome such rejection.

Claim 1 is Patentable Over Agarwal, Ma and Kobayashi

Claim 1 stands rejected under 35 U.S.C. § 103 as obvious in light of the combination of Agarwal *et al.*, *Proceedings of the International Symposium on Power Semiconductor Devices and IC's* (1996) pp. 119-22 (hereinafter "Agarwal"), Ma *et al.*, *J. Vac. Sci. Technol. B.* (Jul/Aug 1993) Vol. 11, No. 4, pp. 1533-40 (hereinafter "Ma") and Kobayashi *et al.*, 1990 Symposium on VLSI Technology, *IEEE*, pp. 119-20 (hereinafter "Kobayashi"). Official Action, p. 2. In particular, the Official Action asserts that Agarwal "teaches a SiC device and suggests in the conclusion that gate dielectrics of alternative insulators of oxide/nitride/oxide material should be investigated." Official Action, pp. 2-3. The Official Action relies on Ma and Kobayashi as disclosing ONO structures "with thickness values in the range claimed." Official Action, p. 3. The Official Action further states that "it would have been obvious to have practiced similar ONO structures in Agarwal to improve dielectric breakdown." Official Action, p. 3.

Initially, Applicants note that the cited Agarwal reference does not disclose ONO structures and, in fact, states the reliability of such structures "needs to be established." Agarwal, Conclusion. Thus, Agarwal does not disclose such structures but merely suggests that such structures should be investigated. Obvious to try is not

the standard for obviousness. There must also be an expectation of success. *See* M.P.E.P. § 2145. Given Agarwal's indication that the reliability of such structures is unknown, clearly there is no such expectation. Furthermore, given the differences between Si and SiC that are expressly identified in Agarwal, merely because ONO structures were investigated in Si would not suggest that such structures would be suitable in SiC. *See e.g.*, Agarwal, p. 120, citing differences between SiC and Si IGBT's and p. 119, citing differences between SiC and Si as to what dictates the long-term time dependent dielectric breakdown of an insulator.

Furthermore, it should be noted that Claim 1 specifically recites that the first oxide layer is formed directly on the SiC layer. In contrast, Ma and Kobayashi relate to structures on a Si substrate. *See* Ma, Fig. 1 and Kobayashi, Section II. Applicants submit that SiC is different from Si and that the underlying layer on which the structure is formed affects the resulting layer. Applicants also submit that one of skill in the art would not look to the Si art for teachings with regard to SiC. Because the characteristics of the structure are, at least to some degree, affected by the characteristics of the crystal interface, the use of a particular configuration in Si would not necessarily be transferable to SiC. Given the crystal differences, operating range differences and physical property differences between SiC and Si, for example, as discussed in Agarwal, use of a particular structure on Si would not suggest the use of such a structure in SiC.

In light of the above discussion, Applicants submit that Claim 1 is neither disclosed nor suggested by the cited references. Accordingly, Applicants request allowance of Claim 1.

Claims 2-21 Are Patentable Over the Cited References

Claims 2-21 stand rejected under 35 U.S.C. § 103 as obvious in light of the combination of United States Patent No. 5,479,316 to Smrtic *et al.* (hereinafter "Smrtic"), PCT Publication No. WO 97/39485 to Slater *et al.* (herein after "Slater"), United States Patent No. 5,739,564 to Kosa *et al.* (hereinafter "Kosa"), Ma and Kobayashi.

Claim 2 specifically recites that the capacitor is on a SiC layer. Neither Smrtic, Slater, Kosa, Ma nor Kobayashi describe a MIM capacitor on a SiC layer. As such, each of the recitations of Claim 2 has not been found in the art. Furthermore,

even if the cited references could be properly combined, such a combination would not result in the claimed structure. For example, the only cited reference that relates to SiC is Slater. However, Slater only describes masks and/or gate oxides as silicon dioxide. Thus, even if the cited references did disclose an ONO structure, the combination of that structure with Slater would result in an ONO mask or an ONO gate oxide. Furthermore, none of the cited references suggest that an ONO capacitor would be capable of withstanding the operating conditions associated with SiC. As acknowledged in the Official Action, the properties of SiC are different from those of Si and the operating conditions for SiC are very different from those of Si. As such, Applicants submit that teachings relating to Si would not be viewed as transferable to SiC. For example, the Agarwal article discussed above clearly indicates that the suitability of ONO for use in SiC structures needs further investigation. Merely because a Si references describes an ONO structure does not indicate that such a structure would be suitable for use in SiC devices. Accordingly, Applicants submit that Claim 2 is patentable over the cited references.

Applicants further submit that Claims 3-12 are patentable as depending from a patentable base claim. However, Applicants also submit that certain of Claims 3-12 are separately patentable over the cited references. For example, Claim 4 recites that the "the first thickness and the third thickness are at least about one order of magnitude smaller than the second thickness." Claim 5 also recites that "the first thickness is from about 10 to about 30 nm, the second thickness is from about 200 to about 300 nm and the third thickness is from about 10 to about 30 nm." However, Ma describes a thickness of 5 nm for the oxide and 5-25 nm for the nitride. *See* Ma, p. 1534. Applicants' review of Kobayashi indicates that Kobayashi does not provide a thickness for the nitride layer and, thus, does not disclose any relationship between the thickness of the oxide layers and a nitride layer. *See e.g.*, Kobayashi, Figure 1. The other cited references either do not describe ONO structures or, to the extent that the term "combinations thereof" is interpreted as describing an ONO structure, give no specifics of layer thickness. *See e.g.*, Smrtic. Thus, Applicants submit that Claims 4 and 5 are separately patentable over the cited references for at least these additional reasons. Should the rejection of Claims 4 and 5 be maintained, Applicants

respectfully request that the Examiner specifically identify where in the cited references the recitations of Claim 4 and Claim 5 are found.

Applicants also submit that Claims 6, 8 and 9 are separately patentable over the cited references. Claim 6 recites that "at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured so that the dielectric structure has a mean time to failure versus voltage characteristic which has a greater slope than a corresponding MIM capacitor with only a nitride dielectric." Claim 8 recites that "at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C." Claim 9 recites that "at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of at least about 100 °C."

The Official Action does not even address the recitations of Claims 6, 8 and 9. Based on Applicants' review of the cited art, it appears that none of the cited references even discuss mean time to failure. Thus, the cited references do not disclose or suggest the recitations of Claims 6, 8 or 9. As such, Applicants submit that the Official Action has failed to establish a prima facie case of obviousness with respect to these claims and, therefore, submit that Claims 6, 9 and 9 are separately patentable for at least these additional reasons. Should the rejection of Claims 6, 8 and 9 be maintained, Applicants respectfully request that the Examiner specifically identify where in the cited references the recitations of Claim 6, Claim 8 and Claim 9 are found.

Independent Claim 13 recites an interconnection structure that includes:

> a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;
>
> a first layer of oxide on the first interconnect layer so as to cover at least a portion of the plurality of regions of interconnection metal;
>
> a layer of dielectric material on the first layer of oxide opposite the first interconnect layer and having a dielectric constant higher than a dielectric constant of the first oxide layer;
>
> a second layer of oxide on the layer of dielectric material opposite the first layer of oxide; and

a second interconnect layer on the second layer of oxide opposite the layer of dielectric material and having a plurality of regions of interconnection metal.

Claim 13. Applicants submit that none of the cited references disclose or suggest using such a structure as an interconnection structure.

The Official Action's only discussion of Claims 13-21 is to state that "the prior art applied shows interconnect metallization and the capacitor structures would be disposed on a layer of oxide on the substrate with overlying dielectric layers." Official Action, p. 4. Applicants submit that none of the cited references disclose the use of the structure of Claim 13 for an interconnection structure. Furthermore, the Official Action has failed to establish where such a structure is disclosed in any of the cited references or how or why the cited references would be modified to result in such a structure. Thus, Applicants submit that Claims 13-21 are patentable over the cited references. Should the rejection of Claims 13-21 be maintained, Applicants respectfully request that the Examiner specifically identify where in the cited references the recitations of Claims 13-21 are found and explain why the cited references would be modified to result in the recitations of Claims 13-21.

While each of Claims 14-21 are patentable as depending from a patentable base claim, Applicants submit that certain of these claims are separately patentable over the cited references. For example, Claims 15-17, 19 and 20 have recitations corresponding to those of Claims 4-6, 8 and 9 and, therefore, are separately patentable over the cited references for at least the additional reasons discussed above.

Claims 33-46 Are Patentable Over the Cited References

Claims 33-46 stand rejected as obvious under 35 U.S.C. § 103 in light of the combination of PCT Publication WO 97/17730 to Lipkin *et al.* (hereinafter "Lipkin"), Smirtic, Slater, Kosa, Ma and Kobayashi. In particular, the Official Action states that "Slater, Kosa, Ma and Kobayashi are applied as above for their suggestions of SiC material benefits, ONO thicknesses, etc. Applicants's claims are obvious structure." Official Action, p. 4.

Claim 33 recites a MIM capacitor with a dielectric having a formula $Si_3N_{4-x}O_X$, where $0<X<1$ as the dielectric material. Applicants submit that Lipkin does not disclose or suggest the use of oxynitride as a MIM capacitor dielectric material.

Lipkin describes a layered dielectric on silicon carbide. *See* Lipkin, Abstract. Lipkin does not describe MIM capacitor structures. Furthermore, Applicants submit that it would be an improper hindsight reconstruction of Smrtic to interpret the reference to "combinations thereof" to disclose both the silicon oxynitride as recited in Claim 33 and an ONO structure as recited in Claims 2-21. With regard to Ma and Kobayashi, neither of these references describe the use of oxynitride but describe ONO structures with silicon nitride as the nitride. Similarly, while Kosa may describe ONO, it does not discuss silicon oxynitride as recited in Claim 33. Thus, Applicants submit that none of the cited references disclose or suggest each of the recitations of Claim 33. Applicants also submit that the references may not be properly combined for the reasons discussed above with regard to Claim 2. Accordingly, Applicants submit that Claim 33 is patentable over the cited references.

Independent Claim 40 recites an interconnection structure where the interconnection structure utilizes silicon oxynitride. Applicants submit that Claim 40 is patentable for reasons analogous to those recited above with reference to Claim 13. Applicants submit that Lipkin does not provide the teachings missing from the other cited references as Lipkin also does not suggest the use of silicon oxynitride in an interconnection structure. Accordingly, Claim 40 is patentable over the cited references.

While each of the dependent claims 34-39 and 41-46 is patentable as depending from a patentable base claim, Applicants submit that certain of the dependent claims are separately patentable over the cited references. For example, Claims 34, 36, 37, 42 and 44 include recitations of the mean time to failure characteristics of the structure. Applicants submit that the Official Action has failed to establish that the cited references disclose structures with such characteristics and, therefore, the claims are separately patentable over the cited references for at least these additional reasons.

Finally, Claim 41 recites that "the layer of dielectric material has a thickness of from about 20 nm to about 400 nm." The Official Action has failed to identify where any of the cited references disclose or suggest the use of a silicon oxynitride layer having the claimed thickness. As such, Applicants submit that Claim 41 is separately patentable for at least these additional reasons.

Conclusion

In light of the above amendments and remarks, Applicant respectfully submits that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s)-including fees for net addition of claims-are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Non-Fee Amendment, Commissioner for Patents, Washington, DC 20231 on July 29, 2002.

Traci A. Brown
Date of Signature: July 29, 2002

VERSION WITH MARKINGS TO SHOW CHANGES

In the Title:

Please amend to title to recite as follows:

HIGH VOLTAGE, HIGH TEMPERATURE CAPACITOR AND INTERCONNECTION STRUCTURES[AND METHODS OF FABRICATING SAME]

In the Claims:

Please cancel the non-elected Claims 22-31 and 47-56.

Please amend Claim 1 to recite as follows:

1. (Amended) A capacitor having a dielectric structure comprising:

a silicon carbide layer;

a first oxide layer having a first thickness directly on the silicon carbide layer;

a layer of dielectric material on the first oxide layer and having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

a second oxide layer on the layer of dielectric material opposite the first oxide layer and having a third thickness; and

wherein the first thickness is between about 0.5 and about 33 percent and the second thickness is between about 0.5 and about 33 percent of the sum of the first, second and third thicknesses.

Please amend Claim 2 to recite as follows:

2. (Amended) [The capacitor of Claim 1, further comprising:] A capacitor having a dielectric structure comprising:

a silicon carbide layer;

a first oxide layer having a first thickness on the silicon carbide layer;

a layer of dielectric material on the first oxide layer and having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

a second oxide layer on the layer of dielectric material opposite the first oxide layer and having a third thickness;

wherein the first thickness is between about 0.5 and about 33 percent and the second thickness is between about 0.5 and about 33 percent of the sum of the first, second and third thicknesses;

a first metal layer on the first oxide layer opposite the layer of dielectric material and disposed between the first oxide layer and the silicon carbide layer; and

a second metal layer on the second oxide layer opposite the high dielectric layer so as to provide a metal-insulator-metal (MIM) capacitor.

Please cancel Claim 32.

Please amend Claim 33 to recite as follows:

33. (Amended) [The capacitor of Claim 32, further comprising] A capacitor comprising:

a silicon carbide layer;

a layer of dielectric material on the silicon carbide layer, the layer of dielectric material comprising silicon oxynitride having a formula $Si_3N_{4-X}O_X$, where $0<X<1$;

a first metal layer on the layer of dielectric material opposite the silicon carbide layer; and

a second metal layer on the layer of dielectric material and disposed between the layer of dielectric material and the silicon carbide layer so as to provide a metal-insulator-metal (MIM) capacitor.